WHAT IS CLAIMED IS:

1. A method for controlling a flash memory, said method including steps of:

receiving a logical address from a host system;

translating the received logical address into a physical address; and

writing data received from the host system into a storage location in the flash memory, said location being addressed by the physical address,

wherein, with the storage location of the addressed flash memory being linked and already written with valid data, the step of writing data includes step for either moving the valid data in the storage location to the linked location if a use ratio of the linked location is greater than a reference value or moving the valid data in the storage location to another linked location if the use ratio of the linked location is less than the reference value.

2. The method as recited in claim 1 further comprising a step for revising a BiT/link table and a ST table for both the storage location and the linked location after the movement of the valid data when the use ratio of the linked location is greater than the reference.

3. The method as recited in claim 1, wherein the reference value is determined that a time in moving data between the locations becomes minimum.

4. A method for controlling operations of flash memory and transmitting data between a host system and the flash memory,

said flash memory including a plurality of memory blocks, each memory block having a plurality of pages/sectors, a data writing operation by the host system to the flash memory being performed in one sector unit, an erase operation to the flash memory being performed in one block unit, and the plurality of memory blocks including basic blocks addressed by physical addresses corresponding to logical addresses transmitted from the host system, first link blocks to which the basic blocks are linked, and second link blocks to which the first link blocks are linked,

said method including steps of:

writing data received from the host system to the flash memory;

moving valid data in the basic block to the first link block when a use ratio of the first link block is greater than a reference value; and

moving valid data in the first link block to the second link block when a use ratio of the first link block is less than the reference value.

5. The method as recited in claim 4 further comprising steps:

revising a BiT/link table and a ST table of the basic and first link blocks, which is performed after the moving step of valid data in the basic block to the first block; and

revising a BiT/link table and a ST table of the basic, first and second link blocks, which is performed after the moving step of valid data in the first block to the second block.

6. An apparatus for controlling a flash memory and transmitting data between a host system and the flash memory,

said flash memory including a plurality of memory blocks, each memory block having

a plurality of pages/sectors, a data writing operation by the host system to the flash memory being performed in one sector unit, an erase operation to the flash memory being performed in one block unit, and the plurality of memory blocks including basic blocks addressed by physical addresses corresponding to logical addresses transmitted from the host system, first link blocks to which the basic blocks are linked, and second link blocks to which the first link blocks are linked,

said apparatus including:

means for writing data received from the host system to the flash memory;

means for moving valid data in the basic block to the first link block when a use ratio of the first link block is greater than a reference value; and

means for moving valid data in the first link block to the second link block when a use ratio of the first link block is less than the reference value.

7. The apparatus as recited in claim 6 further comprising:

means for revising a BiT/link table and a ST table of the basic and first link blocks, when the valid data in the basic block is moved to the first link block; and

means for revising a BiT/link table and a ST table of the basic, first and second link blocks when the valid data in the first link is moved to the second link block.

8. The apparatus as recited in claim 7, wherein the BiT/link table includes a basic block address, a chip address for the basic block, a link block address, a chip address for the link block and data for representing link state.

9. The apparatus as recited in claim 7, wherein the ST table includes data for representing valid data written information and invalid data written information.

10. The apparatus as recited in claim 8, wherein each of the BiT/link table and the ST table is comprised of two memory blocks.

11. The apparatus as recited in claim 6, wherein said means for moving data operates when the host system is in an idle state.

12. An apparatus for controlling a flash memory, which is connected between a flash memory array and a host system and transmits data in a sector unit to the flash memory array,

said flash memory array including a plurality of memory banks, each memory bank including a plurality of memory units, each memory unit including a plurality of memory blocks, each memory block having a plurality of pages, each page including one or more sectors,

said apparatus including:

means for simultaneously enabling, when data received from the host system is two or more sector data for different memory units, said memory units addressed to receive said sector data, so that said two sector data are programmed concurrently into the enabled memory units; and

means for enabling, when data received from the host system is one sector data, one memory unit addressed to receive said sector data and for programming the received sector data into the memory unit.

13. The apparatus as recited in claim 12, wherein the flash memory has a separate bus for chip selection for each of the plurality of memory banks.

14. The apparatus as recited in claim 12, wherein the flash memory has a control signal bus commonly connected to the plurality of memory banks.

15. An apparatus for controlling a flash memory, which is connected between a flash memory array and a host system and transmits data in a sector unit to the flash memory array,

said flash memory array including a plurality of memory banks connected in parallel, each memory bank including a plurality of memory units, each memory unit including a plurality of memory blocks, each memory block having a plurality of pages, each page including one or more sectors,

said apparatus including:

data interface pins of such number that can be connected to the parallel memory banks;

said flash memory controlling apparatus and the flash memory array have in common a control signal interface pin; and

said data interface pin and a chip selection signal pin are connected separately between the flash memory control apparatus and the plurality of memory banks of flash memory array.

16. A method for controlling a flash memory, including steps of:

receiving a logical address for the flash memory from a host system;

translating the received logical address into a physical address;

determining the number of sector that is to be written into the flash memory by the host system;

enabling one flash memory bank corresponding to a bank calculation result, said bank calculation being performed after receiving one sector data when the number of sector is '1';

enabling two flash memory banks when the number of sector is '2' and two sector data is received; and

performing a flash write operation to a memory block of the enabled memory bank, said memory block being addressed by the physical address.